REMARKS

I. Status Summary

Claims 1-10 are currently pending. Claim 1 is amended herein. Therefore, upon entry of this Amendment, Claims 1-10 will be pending.

Element (b) of Claim 1 has been amended to include the phrase "wherein the base address register is switched through by the first multiplexer circuit". Support for the amendment to element (b) of Claim 1 can be found throughout the subject application, particularly at lines 20-28 of page 10.

II. Claim Objections

Claim 1 stands objected to because of informalities. Specifically, the Examiner stated that all occurrences of the phrase "which, in a manner dependent" should be amended to "which, in a manner is dependent". (Official Action, page 2.) Applicants have amended Claim 1 as suggested by the Examiner.

Further, regarding Claim 1, the Examiner stated that the number (61) should be removed from the claim. Applicants have removed the number (61) from Claim 1.

For the above reasons, applicants respectfully submit that the objections to Claim 1 should be withdrawn.

III. Claim Rejections Under 35 U.S.C. § 112

Claims 1-10 stand rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject

matter which applicants regard as the invention. Specifically, regarding Claim 1, the Examiner stated that the phrase "the through-connected base address register" at line 13 and "the through-connected base offset register" at line 16 lack sufficient antecedent basis. (Official Action, page 2.) The Examiner also rejected Claims 2-10 because the claims depend on Claim 1 and include the same problems of insufficient antecedent basis. (Official Action, pages 2 and 3.)

Regarding the phrase "the through-connected base address register" at line 13 of Claim 1, element (b) of Claim 1 has been amended to recite the phrase "wherein the base address register is switched through by the first multiplexer circuit". Applicants respectfully submit that the added phrase provides sufficient antecedent basis for the phrase "the through-connected base address register" at line 13.

Regarding the phrase "the through-connected base offset register" at line 16 of Claim 1, applicants note that the phrase at line 16 reads "the through-connected offset register group". Element (c) of Claim 1 recites "a second multiplexer circuit ... through-connects the offset register group". Thus, Claim 1 recites that the offset register group is through-connected and provides antecedent basis for the phrase "the through-connected offset register group". For this reason, applicants respectfully submit that the phrase "the through-connected offset register group" has sufficient antecedent basis.

Applicants respectfully submit that the amendments to Claim 1 overcome the rejection of Claims 1-10 under 35 U.S.C. §112, second paragraph.

IV. Claim Rejections Under 35 U.S.C. § 103(a)

Claims 1-10 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,657,466 to Yazawa (hereinafter, "Yazawa") in view of U.S. Patent No. 4,779,084 to Tanaka et al. (hereinafter, "Tanaka") and U.S. Patent No. 5,883,905 to Eastburn (hereinafter, "Eastburn"). This rejection is respectfully traversed.

Claim 1 recites an address generator for generating addresses to test an addressable circuit. For example, referring to Figure 3 of the present application, an address generator **1** may be utilized for generating addresses to test an addressable circuit **2**. (Application, page 6, lines 25 and 26.) An exemplary schematic diagram of address generator **1** is shown in Figure 4. Claim 1 recites that the address generator can have at least one base address register (such as one of a plurality of base address registers **12a, 12b**, etc. shown in Figure 4) for buffer-storing a base address. The base address register in each case can be assigned an associated offset register group (such as offset register group **13a** and **13b** shown in Figure 4) having a plurality of offset registers (for example, offset register group **13a** has offset registers **13a-1**, **13a-2**, etc. shown in Figure 4) for buffer-storing relative address values. The address generator can also have a first multiplexer circuit, which, in a manner is dependent on a base register selection control signal, switches through an address buffer-stored in the base address register to a first input of an addition circuit and to an address bus, which is connected to the circuit to be tested. In addition, the address generator can include a second multiplexer circuit, which, in a manner is

dependent on the base register selection control signal, through-connects the offset register group associated with the through-connected base address register to a third multiplexer circuit. The third multiplexer circuit is dependent on an offset register selection control signal, through-connects an offset register of the through-connected offset register group to a second input of the addition circuit. Further, the addition circuit adding the address present at the first input to the relative address value present at the second input to form an address which is buffer-stored in the base address register. Summarily, neither Yazawa, Tanaka, nor Eastburn, alone or in combination, discloses or suggests the features recited by Claim 1.

Yazawa is directed to a circuit for designating write and read addresses of a random access memory (RAM) functioning as a delay circuit in an audio surrounding system. The Yazawa address generator circuit comprises a pointer register **1** which stores a point value for indicating a write and read address of the RAM. (Yazawa, column 3, lines 26-30.) In addition, the address generator circuit includes a write offset register **7** and a read offset register **8** for storing different offset values which indicate an offset from the point value. (Yazawa, column 3, lines 30-33.) A multiplexer **3** is utilized for selecting one of offset registers **7** and **8**. (Yazawa, column 3, lines 33-35.) Further, the outputs of multiplexer **3** and point register **1** are added to generate a write or read address. (Yazawa, column 3, lines 36-38.) In addition, Yazawa teaches that the pointer value of point register **1** is renewed after write and/or read addresses are generated by feeding back the output of an adder **4** to point register **1**. (Yazawa, column 3, lines 55-58.)

As previously stated, Claim 1 recites an address generator having first and second multiplexer circuits. Yazawa fails to disclose or suggest multiplexer circuits as required by Claim 1. The Yazawa multiplexer **3** is utilized for generating a write or read address. (Yazawa, column 3, lines 36-38.) Further, Yazawa teaches that the output of multiplexer **3** is added to the output of point register **3** for generating a write or read address. (Yazawa, column 3, lines 36-38.) Yazawa only discloses a single multiplexer circuit, not two multiplexer circuits as required by Claim 1. Moreover, Yazawa does not disclose or suggest the features of either of the multiplexer circuits recited by Claim 1.

Tanaka fails to overcome the significant shortcomings of Yazawa. Tanaka discloses an address generator for supplying address signals to a display memory for reading out image data stored in the display memory. For example, Figure 1 of Tanaka illustrates a memory address generating circuit **7'** which is a main part of a display control circuit **7** shown in Figure 4. (Tanaka, column 3, lines 21-25.) Circuit **7'** includes a start address register **14** for storing a start address, and an offset register **13** for storing a single offset value. (Tanaka, column 3, lines 25-36.) The offset value is equal to the difference between the width of display memory **4** (shown in Figure 4) and the width of the displayed picture in terms of a display character unit. (Tanaka, column 2, lines 53-64.) In order to display the display area of a CRT display, a start address is set into start address register **14** and a first line is scanned. (Tanaka, column 2, line 65, to column 3, line 2.) When the end of the first line is reached, the offset value is added to the memory address of the terminal point of the first line in

order to get the memory address of the start point of the second line. (Tanaka, column 3, lines 2-6.) To get the start address of the next line to be scanned, the offset value has to be added to the memory address of the terminal point of the preceding line. (Tanaka, column 3, lines 6-9.) The offset is always constant. Display control circuit **7** also includes an adder **20** for adding the offset value to the address of the end of one of the lines of the display. Also, a selector **15** is available to select one of the start address and the address generated by adder **20**. (Tanaka, column 3, lines 34-36.) The start address is only selected by selector **15** at the beginning of the scanning procedure.

The Examiner contended that selector **15** of Tanaka corresponds to the first multiplexer circuit recited by Claim 1. (Official Action, page 4.) Applicants respectfully disagree because the first multiplexer recited by Claim 1 includes features that are lacking in selector **15** of Tanaka. Referring to Claim 1, Claim 1 recites that the first multiplexer circuit switches through an address, namely dependent on a base register selection control signal. According to the teachings of Tanaka, selector **15** is controlled by a selector signal **25**. (Tanaka, Figure 1.) Selector **15** selects start address register **14** when selector signal **25** is set to "0". (Tanaka, column 3, line 67, to column 4, line 4.) This is the case at one line display period just prior to the end of one field of the display. Therefore, selector **15** selects the start address in start address register **14** dependent upon a scanning position within a line of a field of the display, namely just prior to the end of the last line of the field. Therefore, selector **15** cannot select start address register **14** dependent on a selection of the start address

register. In marked contrast, the first multiplexer recited by Claim 1 switches through an address dependent on a base register selection control signal.

Eastburn fails to overcome the significant shortcomings of Yazawa and Tanaka. Eastburn is directed to a pattern generator in automatic test equipment for testing circuits, particularly RAMs or dynamic random access memories (DRAMs). Address generators, namely X, Y, and Z arithmetic logic units (ALUs) (X ALU **160**, Y ALU **140**, and Z ALU **120**), ALUs provide X address, Y address, and Z address output signals to an address scrambler **200**, which may rearrange the signals and subject them to Boolean operations to produce the X, Y, and Z device address signal outputs of the algorithmic test pattern generator, AGP. (Eastburn, column 4, lines 9-26.) Address scrambler **200** comprises a crosspoint multiplexer **201** which receives the X, Y, and Z addresses from the ALUs and connects any of them, one-to-one, to any of its outputs. (Eastburn, column 4, lines 20-26, and Figure 2.)

The Examiner contended that crosspoint multiplexer **201** corresponds to the second multiplexer circuit of Claim 1 and that the ALUs **120**, **140**, and **160** correspond to the offset register group of Claim 1. Applicants respectfully disagree. Claim 1 requires that the second multiplexer circuit through-connects an offset register group, namely dependent on a base register selection control signal. According to Eastburn, ALUs are address generators for generating row and column addresses X and Y of a memory location, and a Z device address or segment. (Eastburn, column 3, lines 40-49.) Applicants submit that the addresses generated

by ALUs **120**, **140**, and **160** are absolute address values, not relative address values as stored in the offset registers required by Claim 1.

Further, Eastburn's crosspoint multiplexer **201** does not select (or through-connect) an offset register group as required by Claim 1. Eastburn's crosspoint multiplexer **201** connects any 32 bits of a 36 bit address at the inputs, one-to-one, to any of its 32 outputs. The function of crosspoint multiplexer **201** may be defined as selecting. However, it appears that crosspoint multiplexer **201** selects arbitrarily, not dependent on a base register selection control signal, as required by Claim 1.

Therefore, for these reasons, applicants respectfully submit that no prima facie case of obviousness exists, and that the teachings of Yazawa, Tanaka, and Eastburn cannot be combined to either teach or suggest each and every element of Claim 1. In addition, applicants submit that even if the teachings of the references could be combined to teach or suggest each and every element of Claim 1, it would not have been obvious to one of ordinary skill in the art to combine the references. For example, the Examiner contended that it would have been obvious to one of ordinary skill in the art to combine Tanaka's start address register **14** and selector **15** into Yazawa's address register to achieve an address generator having the flexibility to select between the two registers for address and offset value selection. (Official Action, page 4.) The address generator according to this combination of Tanaka and Yazawa would be able to add the address from the output of selector **15** of Tanaka with the output of multiplexer **3** of Yazawa. Applicants respectfully submit that it would not have been obvious to one of ordinary skill in the art to combine Yazawa

and Tanaka in this manner. Yazawa teaches an address generator for an audio surrounding system, whereas Tanaka teaches an address generator for reading out image data recorded in a display memory. Applicants submit that it would not have been obvious to combine the teachings of Yazawa's audio surrounding system with the teachings of Tanaka's display memory.

Moreover, applicants submit that even if one of ordinary skill in the art would be motivated to combine Yazawa's audio surrounding system with Tanaka's display memory, it is unlikely that one of ordinary skill in the art would only insert start address register **14** and selector **15** of Tanaka downstream of adder **20** so that the output of adder **20** is selected by selector **15**. As stated above, the Examiner contended that Tanaka's selector **15** corresponds to the first multiplexer circuit of Claim 1, and that Yazawa's adder **4** corresponds to the addition circuit of Claim 1. Applicants submit that if one skilled in the art would be motivated to insert selector **15** of Tanaka into the address generator of Yazawa, selector **15** must be connected to the output of adder **4**. This combination is in contrast to the requirements of Claim 1 because the first multiplexer circuit of Claim 1 is connected upstream to the addition circuit of Claim 1.

The Examiner also contended that it would have been obvious to one of ordinary skill in the art to incorporate Eastburn's crosspoint multiplexer **201** into Yazawa's address generator to connect offset registers **7** and **8**. (Official Action, pages 4 and 5.) Applicants submit that an address generator of this combination of Yazawa and Eastburn would be operable to create a multi-dimensional address.

Further, applicants respectfully submit that it would not have been obvious to one of ordinary skill in the art to combine Yazawa and Eastburn in this manner. Yazawa teaches write offset register set **7** and read offset register set **8**. The offset values stored in register set **7** are utilized for creating a write address WAD, and the offset values stored in register set **8** are utilized for creating a read address RAD. The difference between addresses **WAD** and **RAD** corresponds to a delay time D_0. Therefore, applicants submit that it would not be reasonable to one of skill in the art to connect offset registers **7** and **8** as suggested by the Examiner. Applicants submit that a person of ordinary skill in the art would not incorporate Eastburn's crosspoint multiplexer **201** into Yazawa's address generator in order to connect register sets **7** and **8** because, as a result, any write and read offset values of register sets **7** and **8** at the input of crosspoint multiplexer **201** would be connected, one-to-one, to any of its outputs. As a result, a proper creation of the write and read addresses **WAD** and **RAD** would not be possible. For this reason, applicants submit that one of ordinary skill in the art would not be motivated to combine Yazawa and Eastburn as suggested by the Examiner.

For the reasons provided above, applicants respectfully submit that no prima facie case of obviousness exists, and that the teachings of Yazawa, Tanaka, and Eastburn cannot be combined to either teach or suggest each and every element of Claim 1. In addition, applicants respectfully submit that one of ordinary skill in the art would not be motivated to combine the teachings of Yazawa, Tanaka, and Eastburn as suggested by the Examiner. Therefore, applicants respectfully submit that the

rejection of Claim 1 under 35 U.S.C. § 103(a) should be withdrawn and Claim 1 allowed at this time.

Claims 2-10 depend from Claim 1. Therefore, Claims 2-10 include the features of Claim 1. Thus, the comments presented above relating to Claim 1 apply equally to Claims 2-10. As such, it is respectfully submitted that Claims 2-10 are not obvious in view of the cited references and that the rejections of Claims 2-10 under 35 U.S.C. § 103(a) should be withdrawn and Claims 2-10 allowed at this time.

CONCLUSION

In light of the above amendments and remarks, it is respectfully submitted that the present application is now in proper condition for allowance, and an early notice to such effect is earnestly solicited.

If any small matter should remain outstanding after the Patent Examiner has had an opportunity to review the above Remarks, the Patent Examiner is respectfully requested to telephone the undersigned patent attorney in order to resolve these matters and avoid the issuance of another Official Action.

DEPOSIT ACCOUNT

The Commissioner is hereby authorized to charge any fees associated with the filing of this correspondence to Deposit Account No. **50-0426**.

Respectfully submitted,

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